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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,066	02/27/2004	Behnam Malekkhosravi	2505332-991100	9171

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,066	MALEKKHOSRAVI ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/789,066 and amendment filed on 12/27/2004. Claims 1-20 remain pending in the application.

Claim Objections

2. Claim 13 is objected to because of the following informalities: phrase "such as" should not be in the claim, since it is not sure whether the limitation be part of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-8 and 11-20 are rejected under 35 U.S.C. 102(a/e) as being anticipated by Gheewala et al. (6,617,621).

5. As to claims 1, 6 and 11, Gheewala et al. teach a metal programmable integrated circuit (IC) apparatus and method of manufacture and design using elevated metal layers for design specific customization. The lower metal layers are used to form core cells and to provide power and clocking signals to the core cells. These core cells are

customizable by the designer using only the upper metal layers. This new architecture allow faster turn-around time and fewer mask while keeping the time-to-market advantages of gate array structure (see abstract, summary). The new architecture as taught by Gheewala et al. is prefabricated up to contact layer to allow a user to customize and program the sub-blocks to the user's requirements through metallization (metal programmable IC) (at see col. 10 lines 29-67, col. 11 lines 1-17). A structural multi-project wafer (SMPW) comprising predesigned/validated and prefabricated core cells and a streamlined ID design flow incorporating the SMPW and having no IP integration or floor planning requirements are described at least in col. 10 lines 29-67, col. 11 lines 1-17). Fig. 1 shows a digital system; Fig. 4 shows a metal programmable for use to customize any IC design from a pre-fabricated/validated functional blocks; Fig. 8-11 show layout diagram of predesigned functional blocks for use to customize any IC design. One of the advantages of the new architecture as taught by Gheewala et al. is to improve over full custom design in which the designer does not have a ready and pre-verified library of cells (functional blocks) available to him (col. 1 lines 34-36).

6. As to claims 2-3, 5, 7, 8, Gheewala et al. teach a metal programmable integrated circuit (IC) apparatus and method of manufacture and design using elevated metal layers for design specific customization. Gheewala et al. teach a plurality of functional blocks are arranged in an array structure (col. 4, lines 56-67); the SMPW is pre-fabricated up to contact layer so that a user can customize and program different blocks of the SMPW to the user's requirements (at least see col. 10 lines 29-67, col. 11 lines 1-17, Fig. 8-11). Gheewala et al. teach a metal programmable integrated circuit (IC)

apparatus and method of manufacture and design using elevated metal layers for design specific customization. The metal programmable IC apparatus comprising variety of currently known in the art or later developed (col. 9, lines 58-64, col. 10, lines 21-28, col. 6, lines 56-67, col. 7, lines 1-55). Thus the group of functional blocks as recited in the claim must be included.

7. As to claim 4, Gheewala et al. teach a metal programmable integrated circuit (IC) apparatus and method of manufacture and design using elevated metal layers for design specific customization. The lower metal layers are used to form core cells and to provide power and clocking signals to the core cells. These core cells are customizable by the designer using only the upper metal layers. This new architecture allow faster turn-around time and fewer mask while keeping the time-to-market advantages of gate array structure (see abstract, summary). Thus, the cycle time must be approximately 1-3 months.

8. As to claim 12, Gheewala et al. teach the functional blocks are metal programmable to a user's specific requirement (see at least abstract, field of the invention).

9. As to claim 13, Gheewala et al. teach, in Figs. 8-11, progressively modifying functional block layout in order to meet user's IC design requirements (see description starting col. 12 line 10).

10. As to claims 14-16, Fig. 1 shows a digital system; Fig. 4 shows a metal programmable for use to customize any IC design from a pre-fabricated/validated functional blocks (cell cores or IPs); Fig. 8-11 show layout diagram of predesigned

functional blocks for use to customize any IC design. The advantages of the new architecture as taught by Gheewala et al. is to improve over full custom design in which the designer does not have a ready and pre-verified library of cells (functional blocks) available to him and low costs (col. 1 lines 15-36).

11. As to claims 17-18, Gheewala et al. teach, in Fig. 4, a metal programmable for use to customize any IC design from a pre-fabricated/validated functional blocks (cell cores or IPs) and progressively modifying functional block layout in order to meet user's IC design requirements (see Figs. 8-11 and description starting col. 12 line 10).

12. As to claims 19-20, Gheewala et al. teach a metal programmable integrated circuit (IC) apparatus and method of manufacture and design using elevated metal layers for design specific customization. The lower metal layers are used to form core cells and to provide power and clocking signals to the core cells. These core cells are customizable by the designer using only the upper metal layers. This new architecture allow faster turn-around time and fewer mask while keeping the time-to-market advantages of gate array structure (see abstract, summary). Gheewala et al. teach a metal programmable for use to customize any IC design from a pre-fabricated/validated functional blocks (cell cores or IPs) and progressively modifying functional block layout in order to meet user's IC design requirements. The new architecture as taught by Gheewala et al. is prefabricated up to contact layer to allow a user to customize and program the sub-blocks to the user's requirements through metallization (metal programmable IC) (at see col. 10 lines 29-67, col. 11 lines 1-17). Thus, Gheewala et al. suggest providing multiple packaging and assembly options for SMPW users, where the

options must be chosen from a group of wire bond, flip chip, BGA, plastics and ceramics because they must be used to manufacture and fabricate the IC design.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being obvious over Gheewala et al. (6,617,321).

15. As to claim 9, Gheewala et al. teach a metal programmable integrated circuit (IC) apparatus and method of manufacture and design using elevated metal layers for design specific customization. The lower metal layers are used to form core cells and to provide power and clocking signals to the core cells. These core cells are customizable by the designer using only the upper metal layers. This new architecture allow faster turn-around time and fewer mask while keeping the time-to-market advantages of gate array structure (see abstract, summary). The new architecture as taught by Gheewala et al. is prefabricated up to contact layer to allow a user to customize and program the sub-blocks to the user's requirements through metallization (metal programmable IC) (at see col. 10 lines 29-67, col. 11 lines 1-17). A structural multi-project wafer (SMPW) comprising predesigned/validated and prefabricated core cells and a streamlined ID

design flow incorporating the SMPW and having no IP integration or floor planning requirements are described at least in col. 10 lines 29-67, col. 11 lines 1-17). Fig. 1 shows a digital system; Fig. 4 shows a metal programmable for use to customize any IC design from a pre-fabricated/validated functional blocks; Fig. 8-11 show layout diagram of predesigned functional blocks that are progressively modified in order to customize to meet IC designer's requirements. One of the advantages of the new architecture as taught by Gheewala et al. is to improve over full custom design in which the designer does not have a ready and pre-verified library of cells (functional blocks) available to him (col. 1 lines 34-36). Although, the above teachings do not use similar language as recited in the claims, it would have been obvious to one of ordinary skill in the art the claimed limitations because the progressively modified layout in Figs. 8-11 suggest the last two steps of the claimed limitations. Gheewala et al. also teach his invention provide improvement over full custom IC design in which the designer does not have a ready and pre-verified library of cells available to him (col. 1, lines 34-36). Thus this would suggest the claimed limitation of if one of the plurality of SMPWs meets an IC designer's requirements, proceeding to a streamlined design flow and production because there is no need to modify any metal programmable IC design.

16. As to claim 10, the claimed limitation is also rejected the same as in the above rejection of claim.

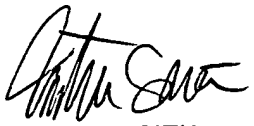
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER